REMARKS

This Amendment responds to the Office Action dated May 18, 2007, in which the Examiner objected to claims 1-20, rejected claims 1-11 and 13 under 35 U.S.C. § 112 second paragraph, rejected claims 1-3, 10-13 and 20 under 35 U.S.C. § 102(e), rejected claims 8-9 and 18-19 under 35 U.S.C. § 103, and objected to claims 4-7 and 14-17 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form.

As indicated above, minor typographical errors in the Specification have been corrected. Applicant respectfully requests the Examiner approve the correction.

As indicated above, minor informalities in the claims have been corrected. Therefore, Applicant respectfully requests the Examiner withdraw the objection to claims 1-20.

As indicated above, claims 1-11 and 13 have been amended in order to more particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Therefore, Applicant respectfully requests the Examiner withdraw the rejection of claims 1-11 and 13 under 35 U.S.C. § 112 second paragraph.

As indicated above, claims 1-2, 8, 10-12, 18 and 20 have been amended in order to make explicit what is implicit in the claims. The amendment is unrelated to a statutory requirement for patentability.

Claims 1-2, 8 and 10 claim a multiplexing apparatus and claims 11-12, 18 and 20 claim a multiplexing method. The multiplexing apparatus and method include generating a plurality of multiplexing instruction data which describe a storage location of each data unit stored in a memory and storing the multiplexing instruction data into the memory in an order that the plurality of data units are to be multiplexed. A multiplex stream is generated by reading the

multiplexing instruction data sequentially from the memory and outputting the data unit corresponding to the multiplexing instruction data.

By having the multiplexing apparatus and method (a) generate a plurality of multiplexing instruction data describing the storage location of each data unit, (b) store the multiplexing instruction data into a memory in an order that the data units are to be multiplexed, (c) generate the multiplexing stream by reading the multiplexing instruction data sequentially from the memory, and (d) outputting a data unit corresponding to the multiplexing instruction data, as claimed in claims 1-2, 8, 10-12, 18 and 20, the claimed invention provides a multiplexing apparatus and method which reduces the processing burden to a CPU since the CPU does not have to transfer an instruction directly to a multiplexer at the time of transfer. The prior art does not show, teach or suggest the invention as claimed in claims 1-2, 8, 10-12, 18 and 20.

Claims 1-3 and 11-13 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Houtepen et al.* (U.S. Publication No. 2002/0012361).

Houtepen et al. appears to disclose in paragraph [0022] a multiplexer 150 comprising a memory structure in which video prepackets and audio prepackets, as received, are stored and from which prepackets are retrieved for outputting. The control unit 140 decides whether an audio prepacket or a video prepacket is to be retrieved and output.

Thus, *Houtepen et al.* only discloses a control unit 140 which instructs a multiplexer 150 to output an audio packet or a video packet. Nothing in *Houtepen et al.* shows, teaches or suggests (a) generating a plurality of multiplexing instruction data which describe a storage location of each data unit in a memory, (b) storing the multiplexing instruction data into the memory in an order that the plurality of data units are to be multiplexed, (c) reading the multiplexing instruction data sequentially from the memory and (d) outputting the data units

corresponding to the multiplexing instruction data stored in the memory as claimed in claims 1, 2, 11 and 12. *Houtepen et al.* teaches away from the claimed invention since the control unit 140 only instructs the multiplexer 150 whether to output the audio prepacket or video prepacket.

Since nothing in *Houtepen et al.* shows, teaches or suggests (a) generating a plurality of multiplexing instruction data which describe a storage location of each data unit in a memory, (b) storing multiplexing instruction data into the memory in an order that the plurality of data units are to be multiplexed, (c) generating a multiplex stream by reading the multiplexing instruction data sequentially from the memory and (d) outputting the data unit corresponding to the multiplexing instruction data stored in the memory as claimed in claims 1-2 and 11-12, Applicant respectfully requests the Examiner withdraw the rejection to claims 1-2 and 11-12 under 35 U.S.C. § 102(e).

Claims 3 and 13 recite additional features. Applicant respectfully submits that claims 3 and 13 would not have been anticipated by *Houtepen et al.* within the meaning of 35 U.S.C. § 102(e) at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraw the rejection of claims 3 and 13 under 35 U.S.C. § 102(e).

Claims 10 and 20 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Zaun et al.* (U.S. Publication No. 2001/0024456).

Zaun et al. appears to disclose an output processor 124 which generates two or more output streams from data stored in packet buffers 104 [0035]. The output processor 124 includes a bus control logic 400 that controls much of the output processor's operation [0036]. The bus control logic 400 generally controls the manner in which the packets are read from the input and insert packet buffers 104, 112 [0038].

Thus, *Zaun et al.* only discloses outputting streams of data by reading packets from packet buffers. Nothing in *Zaun et al.* shows, teaches or suggests (a) generating a plurality of multiplexing instruction data which describe a storage location of each data unit, (b) storing the multiplexing instruction data into a memory in an order that the plurality of data units are to be multiplexed, (c) generating the multiplex stream by reading the multiplexing instruction data sequentially from the memory and (d) outputting the data units corresponding to the multiplexing instruction data stored in the memory as claimed in claims 10 and 20. *Zaun et al.* only discloses a bus control logic which controls the manner that the packets are read from the packet buffers.

Additionally, *Zaun et al.* discloses that the reading process of reading the packets is conducted in three phases including a first phase of reading data other than the packet data itself and second and third phases used to read the stored data [0038]. *Zaun et al.* also discloses that the order that the data is read is based upon the data's priority [0039]. Thus, nothing in *Zaun et al.* shows, teaches or suggests generating a plurality of multiplexing instruction data, storing thereof and generating multiplexing streams by reading the multiplexing instruction data sequentially from a memory. Rather, *Zaun* only discloses reading the data from the memories based upon priority.

Since nothing in *Zaun et al.* shows, teaches or suggests (a) generating a plurality of multiplexing instruction data describing storage locations of each data unit, (b) storing the multiplexing instruction data in an order that the data units are to be multiplexed, (c) reading the multiplexing instruction data sequentially from the memories and (d) outputting the data units corresponding to the multiplexing instruction data as claimed in claims 10 and 20, Applicant respectfully requests the Examiner withdraw the rejection of claims 10 and 20 under 35 U.S.C. §102(e).

Claims 8-9 and 18-19 were rejected under 35 U.S.C. § 103 as being unpatentable over *Dobson et al.* (U.S. Patent No. 6,188,703) in view of *Houtepen et al.*

Dobson et al. appears to disclose a FIFO buffer 32 which signals a MUX microprocessor 22 when sufficient video data is in the buffer 32 (column 3 line 65 - column 4 line 3). Nothing in *Dobson et al.* shows, teaches or suggests generating a plurality of multiplexing instruction data which describe a storage location of each data unit and storing the multiplexing instruction data in an order that the plurality of data units are to be multiplexed as claimed in claims 8 and 18. *Dobson et al.* only discloses signaling a microprocessor when a buffer 32 contains sufficient video data.

Furthermore, *Dobson* discloses that a processor 22 is alerted when there is a video start-code in the transport packet pay load that is about to be read (Col. 4 lines 11-13). Thus nothing in *Dobson et al.* shows, teaches or suggests multiplexing instruction data describing a storage location of each data unit as claimed in claims 8 and 18. Rather, *Dobson et al.* only discloses alerting whether there is a start code in the transport packet.

Additionally, *Dobson et al.* only discloses that the data entry into the buffer 32 is controlled by write logic 41. (Col. 4 lines 42-44). Nothing in *Dobson et al.* shows, teaches or suggests storing a plurality of multiplexing instruction data in a memory as claimed in claims 8 and 18. Rather, Dobson only discloses controlling the data stream entry into the buffer 32.

Also, Dobson discloses multiplexing a time stamp together with audio and video data in packets (Column 3 lines 32-37). Nothing in *Dobson et al.* shows, teaches or suggests reading multiplexing instruction data sequentially from a memory and outputting the data unit corresponding to the multiplexing instruction data in the memory as claimed in claims 8 and 18. *Dobson et al.* only discloses multiplexing a time stamp together with the audio and video data.

As discussed above, *Houtepen et al.* only discloses outputting packets under the control of the control unit 140. Nothing in *Houtepen et al.* shows, teaches or suggests (a) generating a plurality of multiplexing instruction data which describe a storage location of each data unit, (b) storing the multiplexing instruction data into memory in the order that the plurality of data units are to be multiplexed, (c) reading the multiplexing instruction data sequentially from the memory and (d) outputting the data unit corresponding to the multiplexing instruction data stored in the memory as claimed in claims 8 and 18. *Houtepen et al.* only discloses a control unit 140 which decides whether the audio or video prepacket is to be retrieved and output by the multiplexer 150.

A combination of *Dobson et al.* and *Houtepen et al.* would merely suggest that when a buffer 32 has sufficient video data, a microprocessor 22 is signaled, as taught by *Dobson et al.* and the output by a control unit is controlled deciding whether an audio packet or a video packet is to be retrieved as taught by *Houtepen et al.* Thus nothing in the combination of the references shows, teaches or suggests (a) generating a plurality of multiplexing instruction data which describes a storage location of each data unit, (b) storing multiplexing instruction data in an order that the data units are to be multiplexed, (c) reading the multiplexing instruction data sequentially from the memory and (d) outputting the data unit corresponding to the multiplexing instruction data as claimed in claims 8 and 18. Therefore, Applicant respectfully requests the Examiner withdraw the rejection to claims 8 and 18 under 35 U.S.C. § 103.

Claims 9 and 19 recite additional features. Applicant respectfully submits that claims 9 and 19 would not have been obvious within the meaning of 35 U.S.C. § 103 over *Dobson et al.* and *Houtepen et al.* at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraw the rejection of claims 9 and 19 under 35 U.S.C. § 103.

Since objected to claims 4-7 and 14-17 depend from allowable claims, Applicant respectfully requests the Examiner withdraw the objection thereto.

The prior art of record, which is not relied upon, is acknowledged. The reference taken singularly or in combination does not anticipate or make obvious the claimed invention.

CONCLUSION

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 50-0320.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 50-0320.

Respectfully submitted,

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